A MINIATURE LOW CURRENT GaAs MMIC DOWNCONVERTER FOR Ku-BAND BROADCAST SATELLITE APPLICATIONS

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ABSTRACT

A miniature low current GaAs MMIC downconverter with a novel image rejection filter has been developed for commercial Ku-band broadcast satellite receivers. The current consumption of the MMIC downconverter was only 40 mA. The chip size of the MMIC downconverter with the image rejection filter is 1.7 mm × 2.05 mm, which is believed to be the smallest size ever reported.

INTRODUCTION

We previously reported a GaAs MMIC family for Ku-band broadcast satellite applications [1]. This MMIC family consisted of a low noise RF amplifier (LNA), image rejection filter (IRF), mixer, and intermediate frequency amplifier (IFA). The matching circuits of the LNA and filter were composed of coplanar waveguide (CPW), the matching circuits of the mixer were composed of CPW and lumped LC circuits, and the matching circuits of the IFA were composed of lumped LC circuits. The chip size of the IRF was greatly reduced to 0.6 mm × 0.8 mm by using a novel bridged-T band-stop filter configuration. To achieve further reduction of the MMIC downconverter, reduction of the size of the active circuits was required.

We have, therefore, successfully reduced the size of these active circuits (LNA, mixer, and IFA) to less than one half of the previous ones [1] without degrading the RF performance by modifying the CPW and lumped circuits. Furthermore, we have fabricated a miniature single chip MMIC downconverter by using this novel LNA, mixer, and IFA, and a revised IRF.

MMIC DESIGN

A circuit schematic and a photograph of the MMIC downconverter are shown in Figure 1 and Figure 2, respectively. The LNA, IRF, mixer, and IFA are integrated on this MMIC. This MMIC uses 0.3 μm gate ion-implanted GaAs MESFETs. The individual circuit designs and performance are described as follows.

LOW NOISE AMPLIFIER

The LNA consists of two stages in cascade. To reduce the size of the LNA, the line width of the CPW in the interstage and output matching circuits has been reduced to 10 μm, and an interdigitated gate FET has been used in the second stage. The multi-feed T-gate FET in the first stage and the line width of the CPW in the input matching circuit have remained unchanged to maintain low noise performance. The chip size of the LNA is 1.2 mm × 1.2 mm, which is 50% smaller than the one reported previously. The measured RF performance of the LNA is shown in Figure 3. Less than 2.5 dB noise figure and more than 16.5 dB gain have been achieved in the frequency range from 11.7 to 12.2 GHz.

IMAGE REJECTION FILTER

The IRF consists of a high-pass type tee circuit and a bridged transmission line, as shown in Figure 1 and Figure 2. This circuit configuration functions as a band-stop filter [1]. More than 30 dB image rejection ratio has been achieved by adjusting the stop band of the filter to the image frequency. The size of the IRF is 0.5 mm^2, which is much smaller than the other kinds of filters such as a quarter-wavelength coupled line filter.

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MIXER

The mixer has a drain LO injection configuration which does not require an RF-LO combiner and consumes no DC current. To reduce the size of the mixer, the RF, IF, and LO matching circuits consist of lumped LC elements, including spiral inductors and metal-insulator-metal (MIM) capacitors. Self-resonance of the spiral inductor (L1) has been intentionally used to improve the LO-IF isolation and the LO injection efficiency. The IF signal is effectively transmitted to the IF port owing to the series resonance of L1 and C1. The size of the mixer is 0.73 mm × 0.93 mm, which is 50% smaller than the one reported previously. The measured RF performance of the mixer is shown in Figure 4. Less than 6.5 dB noise figure and more than 0 dB conversion gain have been achieved in the frequency range from 11.7 to 12.2 GHz and the corresponding IF frequency range from 1.0 to 1.5 GHz. The LO frequency and input power were 10.7 GHz and 8 dBm, respectively. This performance compares favorably with other mixers composed of distributed elements [2], [3].

INTERMEDIATE FREQUENCY AMPLIFIER

To reduce the size of the IFA, all of the matching and gain blocks are composed of FETs and MIM capacitors, and no spiral inductors. The input matching block is composed of a common gate FET, the gain block is composed of a four stage common source FET in cascade, and the output matching circuit is composed of a common drain FET. The total gate width is 540 μm, which was optimized by using a harmonic balance simulator to simultaneously achieve high linearity and low current. The size of the IFA is 0.65 mm × 1.65 mm, which is 62% smaller than the one reported previously. The measured RF performance of the IFA is shown in Figure 5. More than 24 dB gain has been achieved in the frequency range from 1.0 to 1.5 GHz, at an operating current of only 18 mA (@ Vd = 5 V).

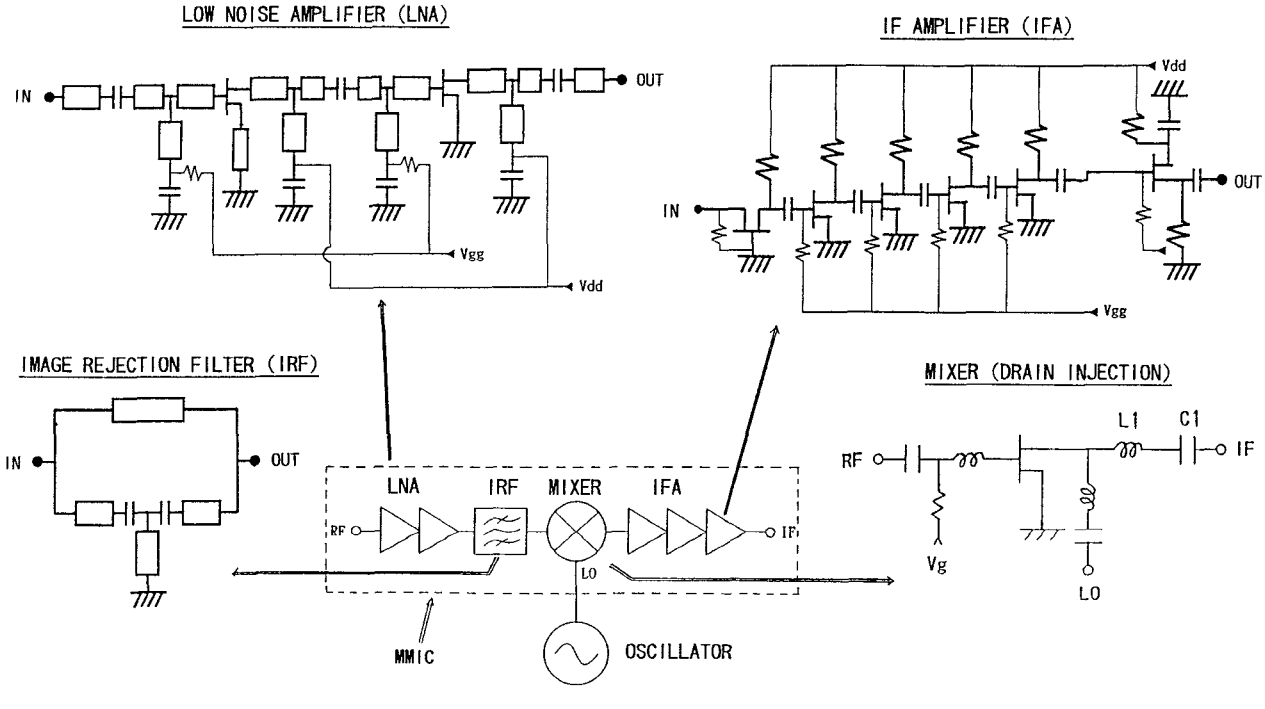

Figure 1. Circuit schematic of the MMIC downconverter.

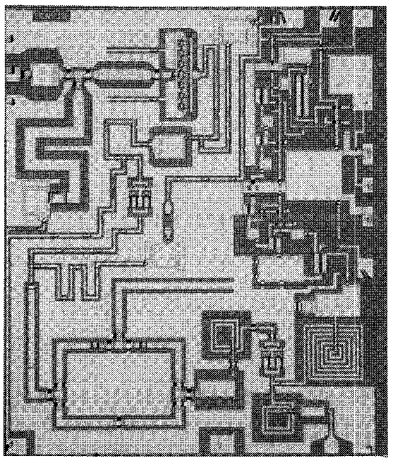

Figure 2. Photograph of the MMIC downconverter.

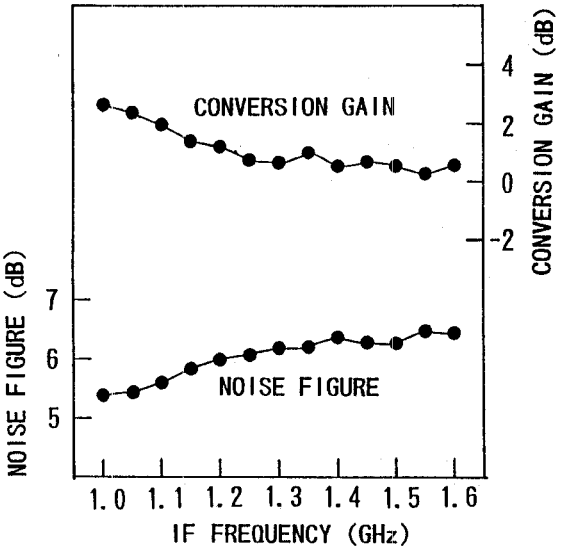

Figure 4. Measured frequency response of the mixer.

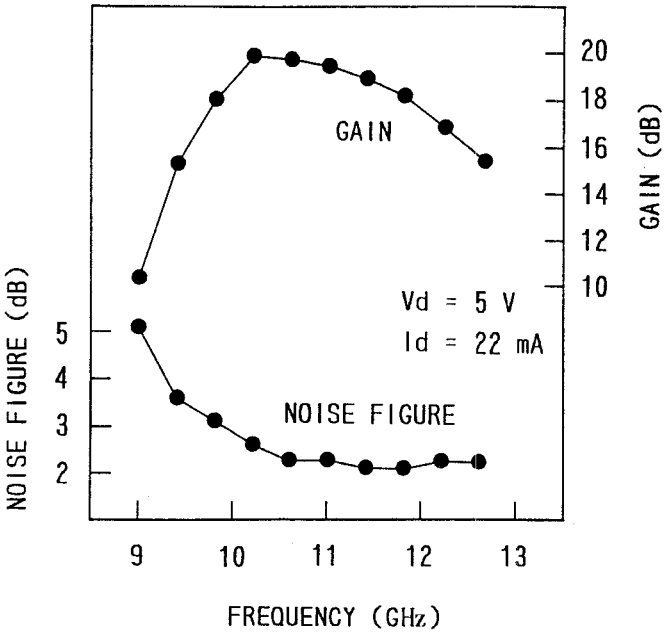

Figure 3. Measured frequency response of the low noise amplifier.

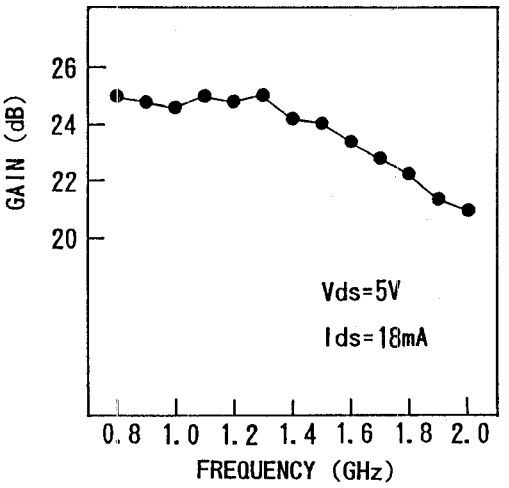

Figure 5. Measured gain of the intermediate frequency amplifier.

MMIC DOWNCONVERTER

As shown in Figure 2, the MMIC downconverter is composed of the LNA, IRF, mixer, and IFA described above. The chip size of the MMIC downconverter is only 1.7 mm × 2.05 mm. The measured conversion gain of the MMIC downconverter is shown in Figure 6. More than 36 dB conversion gain has been achieved in the RF frequency range from 11.7 to 12.2 GHz and the corresponding IF frequency range from 1.0 to 1.5 GHz, at an operating current of only 40 mA.

CONCLUSION

A miniature low current MMIC downconverter has been developed for commercial Ku-band broadcast satellite receivers. The MMIC downconverter receives 11.7 - 12.2 GHz signals and converts them down in frequency to 1.0 - 1.5 GHz with a conversion gain of more than 36 dB. The chip size of the MMIC downconverter with the high performance image rejection filter is 1.7 mm × 2.05 mm, which is believed to be the smallest size ever reported.

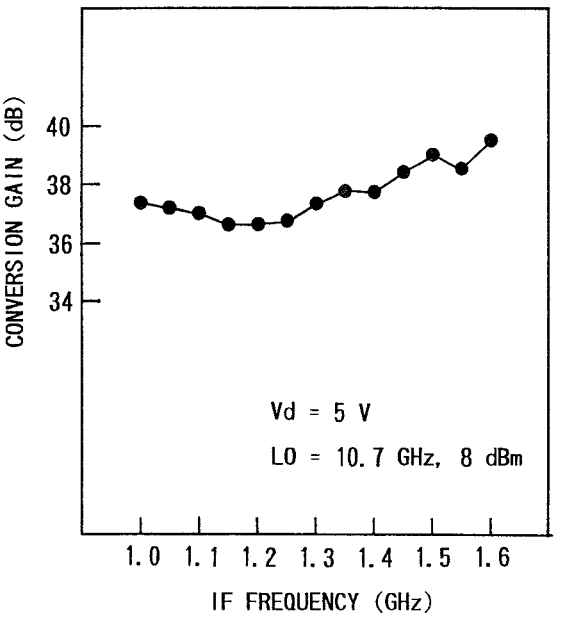

Figure 6. Measured conversion gain of the MMIC downconverter.

ACKNOWLEDGEMENTS

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